REMARKS/ARGUMENTS

Claims 1-22 are pending.

Claim 1 is amended to clarify that the first scanning means comprises a pixel selecting circuit 2 and a switch circuit 3, the second scanning means comprises a pixel selecting circuit 7 and a switch circuit 8, and that a buffer means is provided. Support for this amendment is found throughout the specification, for example, at paragraphs [0013], [0014], [0029] and [0030], and Figs. 4, 6 and 7.

Claims 3 and 4 are amended to depend from claim 1.

Claim 14 is amended to clarify that the method includes temporally storing pixel sensor signals. As with claim 1, support is found throughout the specification, for example, at paragraphs [0013], [0014], [0029] and [0030], and Figs. 4, 6 and 7.

Claims 2, 7-13, and 18-22 are canceled.

Applicant points out that various technical features of certain embodiments of the first scanning means, the second scanning means and the buffer circuit are considered in the specification. In particular, a pixel selecting circuit is provided for providing signals for sequentially selecting sensor signals B1, B2 for one block and a switch circuit is provided for outputting sensor signal B1, B1 by sequentially turning ON analog switches T1, T2 respectively. A bias voltage circuit 9 is also provided for converting respective sensor signals of one pixel block into respective voltage values by a reference resistance with a bias voltage Vcc applied thereto. Each signal lines "a" and "b" is provided with a special buffer circuit 10 with a buffer amplifier BF connected thereto so as to temporally store therein voltage signals Vo read from respective pixels. The voltage signals are then sequentially output from the buffer circuit 10 by switching ON analog switches T1 and T2 respectively from the pixel selecting circuit 7.

Rejections under 35 USC § 112

The rejection of claims 3, 4 and 15 as indefinite is respectfully traversed. These claims, as well as claim 1 and the other remaining claims in the application, are distinct and definite.

The Office Action asserts that the definitions in claim 2 are contradictory with definitions of "the first scanning means" and "the second scanning means" in claim 1. The specification describes in paragraph [0014] the constituent features "...by using a first scanning means for sequentially reading out sensor signals on a block-by-block basis in an order starting from the first block, a buffer means for temporally storing sensor signals in each of the readout blocks and a second scanning means for sequentially reading out pixel signals stored in the buffer means."

The specification also describes in paragraph [0032] that "[i]n this embodiment, each of signal lines "a" and "b" is provided with a special buffer circuit 10 with a buffer amplifier BF connected thereto so as to temporally store therein voltage signals Vo read from respective pixels. The voltage signals are then sequentially output from the buffer circuit 10 by switching ON analog switches T1 and T2 respectively from the pixel selecting circuit 7."

Furthermore, the specification describes in paragraph [0036] that "[a] line of pixels D11~D116 is selected by a pixel line selecting signal LS1 and then analog switches SW1~SW16 are turned ON sequentially according to pixel selecting signals DS1~DS16, thereby sensor signals B1 from odd-numbered pixels (D11, D13, ..., D115) are read out through a signal line "a" and sensor signals B2 from even-numbered pixels (D12, D14, ..., D116) are read out through a signal line "b". The sensor signals B1 and B2 through the signal lines "a" and "b" are converted into respective voltage signals by a bias circuit 9 and then the sensor voltage signals Vo from respective pixels D11~D116 are output in a time series by alternately switching ON and OFF analog switches T1 and T2 according to pixel selecting signals from the pixel selecting circuit 7."

Therefore, a pixel line selecting signal LS1 is output by "a pixel line selecting circuit 1" of "the first scanning means" to select a line of pixels and selecting signals DS1~DS16 are output from the pixel selecting circuit 2 to be read into signal lines "a" and "b". Then, the analog switches T1 and T2 of a switching circuit 8 are tuned ON and OFF according to selecting sensor signals B1 and B2 from "the pixel selecting circuit 7" of "the second scanning means."

From the above description, it is apparent that the first scanning means includes reference number 2, and the second scanning means includes reference number 7.

Rejections under 35 USC § 103

The rejection of claims 1, 5, 6, 14,16 and 17 as obvious over Kimata in view of Hedges, and variously in view of Nomura and in view of Shinotsuka is respectfully traversed. "To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." *In re Royka*, 490 F. 2d 981, 180 USPQ 580 (CCPA 1974); MPEP § 2143.03. In the present case, the prior art does not meet this standard.

Kimata discloses a solid-state image take-up device which can comprise an increased number of pixel lines with an increased number of pixels and in this case requires provision of additional buffer amplifiers one for each of the added pixel lines, resulting in considerable increase in power consumption of the image sensor device. As described for the prior art in the specification of the present application, the construction of an exemplary conventional device has to supply power to a number of buffer amplifiers provided for respective output circuits of pixels per line, thereby considerably increasing the power consumption of the device. In other words, the device is constructed to read sensor signals from respective pixels and convert the signals into corresponding voltage signals by bias circuits having a reference resistance with a biased voltage applied thereon and then temporally store the voltage signals in buffer amplifiers of the buffer circuits connected to the outputs of the respective bias circuits and output the stored voltage signals representing respective pixels from the respective buffer circuits by switching on the respective buffer amplifiers. This device

can attain high signal-driving ability and can thereby read out pixel signals by scanning at an increased speed. However, this device has to turn on a number of reference resistances and buffer amplifiers disposed on the output sides of respective pixel lines, thereby increasing power consumption of the device.

Nomura discloses a device having a bias circuit (output amplifier) which is not a circuit for reading pixels in one block but a circuit for sequentially amplifying respective pixel signals. In other words, the device involves the need of sequentially amplifying sensor signals readout from one block of pixels so that sequentially readout sensor signals can be output as voltage signals defined by applying a bias voltage through reference resistance.

However, this device has low signal-driving ability and therefore cannot realize high-speed reading-out of signals.

Accordingly, the present invention provides a device which can read out sensor signals by high-speed scanning and, at the same time, can effectively prevent increasing the power consumption.

For this purpose, a device according to the present invention evenly divides a line of pixels into a plurality of blocks each containing a given number of pixels and works by sequentially reading-out of pixel signals by a first scanning means for sequentially reading pixel signals on block-by-block basis in the order starting from the first block, temporally storing the readout sensor (pixel) signals in a buffer means and then sequentially reading from the buffer means by using a second scanning means.

With regard to rejection 4 of the Office Action, Hedges is recited as describing "camera and method of controlling a camera and focuses on an optical line array sensor and specifically teaches that the length of the pixel line is divided in n number of groups with each group containing m pixels." However, Hedges merely describes solid-state take-up elements each representing a unit pixel can be arranged to form a matrix of m x n pixels as described in the specification of the present application. Namely, Hedges discloses the arrangement of 100 pixels in one line which is not divided into blocks each

containing a given number of pixels. Therefore, the cited document Hedges is different and does not disclose the present invention.

Double-Patenting Rejection

The current claims are patentably distinct from the cited U.S. Patent No. 7176435. Therefore, Applicant submits that the double-patenting rejection should be withdrawn.

In view of the foregoing amendments and remarks, Applicant submits that the present application is in condition for allowance. A Notice of Allowance is therefore respectfully requested.

A Petition and fee for a 1 month extension of time is being submitted with this response.

No other fee is believed due. However, the Commissioner is hereby authorized during prosecution of this application and any related appeal, to charge any fees that may be required (except for patent issue fees required under 37 CFR §1.18) or to credit any overpayment of fees to Deposit Account No. **50-0337**. Please ensure that Attorney Docket No. **7272-132/10314101** is referred to when charging any payments or credits for this case. If a further extension of time is required in connection with this paper, please consider this a Petition therefor and charge any fees required to Deposit Account No. **50-0337**.

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Respectfully submitted,

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